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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,221	04/13/2004	Se-Hoon Oh	5649-1228	4644
20792	7590	07/13/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			GURLEY, LYNNE ANN	
PO BOX 37428				
RALEIGH, NC 27627			ART UNIT	PAPER NUMBER

2812

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

**Office Action Summary**

Application No.

10/823,221

Applicant(s)

OH ET AL.

Examiner

Lynne A. Gurley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 9-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.


**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
LYNNE A. GURLEY

PRIMARY PATENT EXAMINER  
TC 2800, AU 2812

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of claims 9-27 in the reply filed on 4/11/05 is acknowledged. Claims 1-8 and 28-33 have been canceled.

### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Priority***

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 9-10 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 2004/0262661, dated 12/30/04, filed 3/23/04).

The applied reference has a common assignment and a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Kim shows the method as claimed in figures 1-12 and corresponding text, with buried contact plug 130a on cell array region A; resistor 130b on peripheral circuit region B; first pad contact plug (the part of 130a above the 110 which includes 150a/160a); second pad contact plug 150b/160b; and ohmic layer 140a between the first pad contact plug and the buried contact plug, and 140b between the second pad contact plug and the resistor. The capacitor 200a/220/230 is formed. Etch stop layer 170 is shown. Barrier layer 150a/b is shown.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

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2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 11-14 and 18-27 are rejected under 35 U.S.C. 103(a) as being obvious over Kim et al. (US 2004/0262661, dated 12/30/04, filed 3/23/04) in view of the admitted prior art (specification, figure 1 and pages 1-2).

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a

terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Kim shows the method as claimed and as described in the preceding paragraphs.

Kim lacks anticipation only in not teaching that the a first interlayer dielectric layer is formed on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively; forming a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and forming a metal contact plug in the metal contact hole in the peripheral circuit region; and, forming an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer; forming a first and second adhesion layers.

The Admitted prior art teaches a conventional method of forming a first pad contact hole in the cell array region and a second pad contact hole in the peripheral region wherein first and second pad contact plugs are disposed in the first and second pad contact holes, respectively.

It would have been obvious to one of ordinary skill in the art to have had a first interlayer dielectric layer be formed on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively,

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with the motivation that this is conventionally known in the art as shown by the Admitted prior art and as referred to as the conventional recess process in Kim [0036].

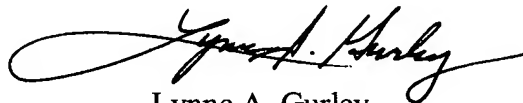
It would have been obvious to one of ordinary skill in the art to have formed a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and to have formed a metal contact plug in the metal contact hole in the peripheral circuit region; and, to have formed an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer; and to have formed a first and second adhesion layer, with the motivation that these are subsequent processing steps which would allow connection to surrounding devices, aid in the reliability of the structure and improve the etching profile of the structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley  
Primary Patent Examiner  
TC 2800, Art Unit 2812

LAG  
July 8, 2005